# SCNAP5 User's Guide

Version 1.1

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## 1. Introduction

SCNAP5 is an extension of SCNAP4 [1] with the enhancement to time domain analysis of both periodic and non-periodic sampled-data analogue networks. It is designed to run under the CADENCE socket environment for mixed-mode simulation, hence part of this manual relates to mixed-mode simulation and users are referred to the appropriate CADENCE document [2]. Many highly efficient techniques which were so effectively used in SCNAP4 have been incorporated. Switches are allowed to be controlled by either external periodic clock signals or internally generated non-periodic digital logic. The nonideal effects such as gain and bandwidth product of opamps and switch resistance can be investigated exactly. The program is written in C.

## 2. How to run SCNAP5

For mixed-mode simulation purposes, SCNAP5 allows a series of command line options which permit it to be used as either a master simulator or as a slave simulator.

(a) SCNAP5 as master

General form:

```
isc -'scnap5 -mixmod -slave<slave command line> -slvhost<name> -shellhost<name>
        -shellport<name> -mmdebug <file>'
```

Example:

```
isc -'scnap5 -mixmod -slave"verilog.vmx +vmxcconfig.vmx test.v"
        -shellhosthogmanay.elec -shellport1312 -mmdebug test.in'
```

| option | function |
|---|---|
| mixmod | Indicates a mixed-mode simulation |
| slave | Indicates the name of slave simulator and any required command line |
| slvhost | Indicates the hostname of slave and is only needed if the slave is running on a seperate machine |
| shellhost | Indicates the name of the machine where ISC † is running |
| shellport | Indicates the socket port that the ISC has opened |
| mmdebug | Flag that turns on the ISC side of the IPC ‡ debug |

† ISC stands for **I**nteractive **S**imulation **C**ontrol

‡ IPC stands for **I**nter **P**rocess **C**ommunication

(b) SCNAP5 as slave

General form:

isc -'scnap5 -mixmod -host<name> -sport<name> -shellhost<name> -shellport<num> -mmdebug <file>'

Example:

isc -'scnap5 -mixmod -hosthogmanat.elec -shellhosthogmanay.elec -shellport1432 -mmdebug test.in'

| option | function |
|---|---|
| mixmod | As in above table |
| host | Indicates the name of the machine where the master simulator is running |
| sport | Indicates the socket port that the master has opened |
| shellhost | As in above table |
| shellport | As in above table |
| mmdebug | As in above table |

## 3. Element description

The input format of SCNAP5 is very similar to that of SPICE and is of the free format type. The first line of the input file must be a title line, and the last line must be a **.end** card. The order of the remaining lines is arbitrary. SCNAP5 is not case-sensitive.

### 3.1 Resistor

General form:

**rxxxxxx node1 node2 val**

Examples:

r1 1 2 100
rin 7 3 4.7k

**node1** and **node2** are the two nodes to which the element is connected. **val** is the resistance value and may be positive or negative but not zero. If the resistance is greater than 1E30, the conductance will be set to zero.

### 3.2 Capacitor

General form:

**cxxxxxx node1 node2 val**

Examples:

c1 1 2 100pf

cb 7 3 4.7nf

**node1** and **node2** are the two nodes to which the element is connected. **val** is the capacitance value and can be positive, negative or zero.

## 3.3 Inductor

General form:

**lxxxxxx node1 node2 val**

Examples:

l1 1 2 100mH

la 2 3 4.55e-3

**node1** and **node2** are the two nodes to which the element is connected. **val** is the inductance value and could be positive, negative or zero.

## 3.4 Switch

General form:

**sxxxxxx node1 node2 clknam [ron = val [roff = val]]**

Examples:

```
s1 4 7 even
sa 2 3 clk1 ron = 4.7k
s7 8 5 odd ron = 5.7k roff = 4Meg
```

**node1** and **node2** are the two nodes to which the element is connected. **clknam** is the name of the clock waveform which controls the switch and must be defined elsewhere. **ron/roff** are optional switch on and off resistances respectively. If the values are not specified then default values are assumed. The default values can be specified by using the option card. However, they cannot override the values which have been set in element card.

## 3.5 Linear Dependent Sources

SCNAP5 allows circuits to contain linear dependent sources. They are characterised by any of the four following equations

$I = G*V \quad V = E*V \quad I = F*I \quad V = H*I$

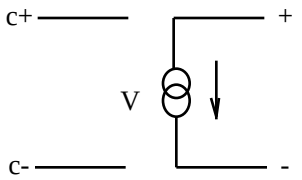
where G, E, F and H are constants representing transconductance, voltage gain, current gain and transresistance, respectively.

## 3.5.1 Linear Voltage-Controlled Current Source

General form:

**gxxxxxx cnode+ cnode- node+ node- val**

Examples:




g1 2 0 5 0 0.1mmho

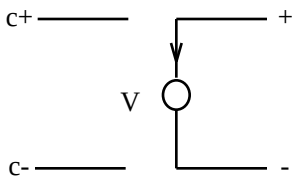
**node+** and **node-** are positive and negative source nodes, respectively. Current flow is through the source from the positive node to the negative node. **cnode+** and **cnode-** are the positive and negative controlling nodes, respectively. **val** is the transconductance value.

## 3.5.2 Linear Voltage-Controlled Voltage Source

General form:

**exxxxxx cnode+ cnode- node+ node- val**

Examples:




e1 2 3 5 1 100k

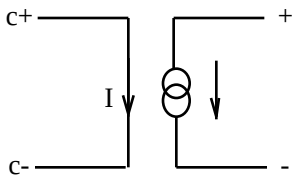
**node+** and **node-** are positive and negative source nodes, respectively. **cnode+** and **cnode-** are the positive and negative controlling nodes, respectively. *Note: (**node+** , **node-**) should not be be the same nodes as (**cnode+**, **cnode-**) except for a ground node.* **val** is the voltage gain.

### 3.5.3 Linear Current-Controlled Current Source

General form:

**fxxxxxx node+ node- vname val**

Examples:




f1 4 7 vz1 5.0

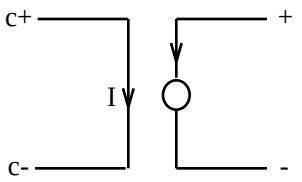
**node+** and **node-** are positive and negative source nodes, respectively. Current flow is through the source from the positive node to the negative node. **vname** is the name of controlling source through which the controlling current flows. The controlling source can be a voltage source, or a voltage-controlled voltage source, or a current-controlled voltage source or an inductor. The direction of positive controlling current is from the positive controlling node, through the source, to the negative controlling node. **val** is the current gain.

### 3.5.4 Linear Current-Controlled Voltage Source

General form:

**hxxxxxx node+ node- vname val**

Examples:




h1 5 17 vz1 0.5k

**node+** and **node-** are positive and negative source nodes, respectively. **vname** is the name of controlling source through which the controlling current flows. The controlling source can be a voltage source, or a voltage-controlled voltage source, or a current-controlled voltage source or an inductor. The direction of positive controlling current is from the positive controlling node, through the source, to the negative controlling node. **val** is the transresistance value.

## 3.6 Independent Sources

General form:

**vxxxxxx node+ node- [source function]**

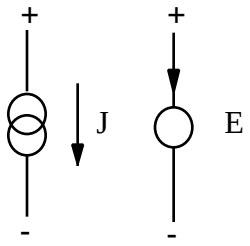
**ixxxxxx node+ node- [source function]**

Examples:

vin 1 0 dc 5.0v

vs 7 3 step 1.0v

isrc 4 9 sin 0.0 100mA 5kHz




**node+** and **node-** are positive and negative source nodes, respectively. For a voltage source, positive current is assumed to flow from the positive node, through the source and out from the negative node. A current source of positive value will force current to flow from the **node+**, through the source and from the **node-**.

## 3.7 Source function

For time-domain analysis, no restrictions are put on the number of independent sources. A source function must be specified for each source and five of these are available in SCNAP5:

### 3.7.1 Step function

General form: **step val**

Examples:

vin 1 0 step 0.1v

isrc 3 7 step 10mA

### 3.7.2 Impulse function

General form: **impulse val**

Examples:

vs 1 0 pulse 3v

is 3 7 pulse 120mA

### 3.7.3 DC source

General form: **dc val**

Examples:

vin 1 0 dc 5.0v

isrc 3 7 dc 3mA

### 3.7.4 Sinusoidal

General form: **sin vo va freq**

Examples:

vs 1 0 sin 0.1v 1.0v 10kHz

isrc 3 7 sin 0 20mA 98kHz

The function is defined as **vo + va*sin(two*pi*freq*time)**

### 3.7.5 Square wave

General form: **pulse v1 v2 td tr tf tw per**

Examples

vin 1 0 pulse -1 1 0 8u 8u 984u 2ms

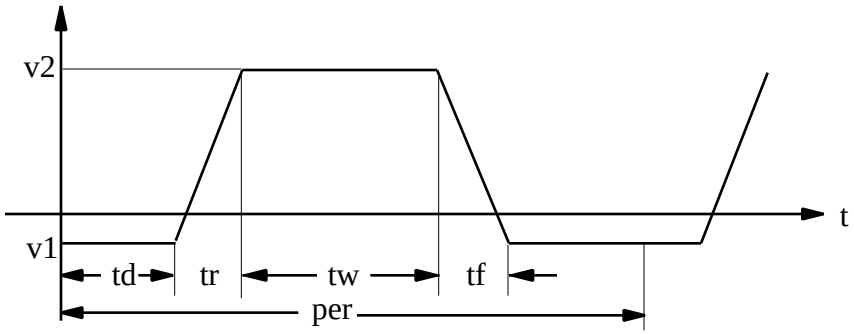



Fig. 1 Square waveform definition

## 4. Comparator

General form:

**kxxxxxx in+ in- clknam [vref = val [ voff = val]]**

Examples:

k1 10 0  99 clk1

ka 0 net7 net99 phi1

**in+** and **in-** are the two input node names of the comparator. **out** is the output node name and should be the same as defined in **.a2d** card. **clknam** is the name of the clock waveform which controls the comparator and must be defined elsewhere. The comparator only changes its output at the rising edge of the controlling clock signal. **vref** is the reference voltage and **voff** is the offset voltage associated with node **in+** (has not been implemented yet!)

## 5. The clock description

To describe the clock signals that control the switches of the network, the **.phase** card is used.

General form:

For periodic clock signal

**.phase clknam pwl time0 v0 [[[time1 v1] time2 v2] ...]**

For non-periodic clock signal

**.phase clknam d2a t1 v1 t2 v2**

Examples:

.phase clk1 pwl 0us 0v 5us 1v 10us 0v

.phase clk2 pwl 0us 1v 10us 0v 20us 1v

.phase phi1 d2a 0us 0v 0.3ms 5v

The **clknam** is the clock name that controls switches. **pwl** is a key word which means that the clock waveform is periodically repeated and described in a piecewise linear manner. It is defined by pairs of numbers (time and value) for each of the breakpoints in a waveform. Each waveform need only be described over one complete period, irrespective of the periods of other clocks of the whole system. The value associated with each time is the value of the waveform at the instant immediately after that time. **d2a** is the key word which means that the clock waveform is determined by digital to logic events. (**t1, v1**) and (**t2, v2**) are pairs of breakpoints in a waveform which only serves as an initial condition and will be overridden during the simulation. It should be stressed that the **clknam** should be defined elsewhere in **.d2a** card.

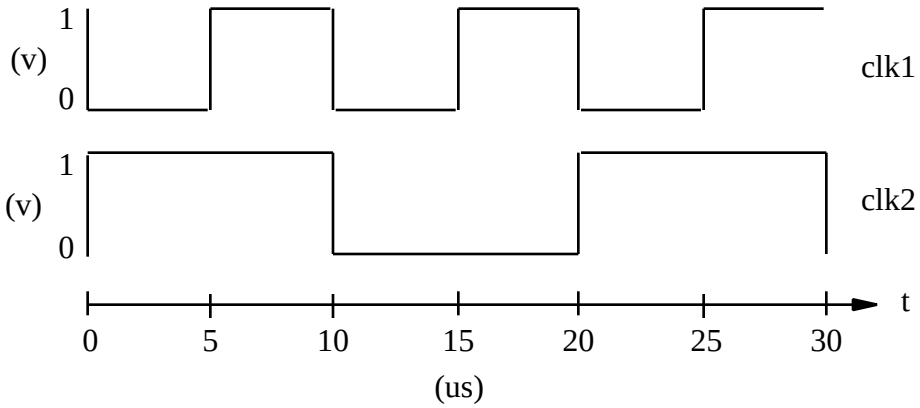



Fig. 2 Clock waveform definition

# 6. Interface nodes between analogue and digital network

## 6.1 Analogue to digital node

General form:

**.a2d dout ain vl vh tx**

Example:

.a2d 99999 net99 0v 5v 0us

This card starts with **.a2d** which defines an analogue to digital node. **dout** is the interface node name which is known by the digital simulator. **ain** is the node name which describes the same node known to SCNAP5. **vl** and **vh** are low and high voltage levels, respectively, the node will be automatically translated to digital "0" or "1" correspondingly. **tx** is the length of time that it takes a node voltage to transit between **vl** and **vh**, in our situation, **tx** is usually set to zero.

## 6.2 Digital to analogue node

General form:

**.d2a din clknam vl vh tr tf**

Examples:

.d2a 99998 clk1 0v 5v 0us 0us

.d2a 99997 clk2 0v 5v 0us 0us

This card begins with **.d2a** which indicates a digital to analogue node. **din** is the node name known by digital simulator. **clknam** is the clock name which controls some switches in the analogue circuit. **vl** and **vh** are the low and high voltage levels which describe the clock waveform and should be greater than or equal to zero. **tr** and **tf** are the rise and fall times of the transition. Since SCNAP5 only allows ideal clock waveforms, **tr** and **tf** are normally set to zero.

## 7. Subcircuit

SCNAP5 provides a powerful subcircuit facility. A subcircuit can be formed with any elements supported by SCNAP5.

### 7.1 Subcircuit definition

General form:

**.subckt subnam node1 [node2 node3 ...] [(parm1 [parm2 parm3 ...])]**

Examples:

.subckt opamp 1 2 3 4 (rin, rout, gain)

Subcircuit definition starts from **.subckt** card. **subnam** is the name of the subcircuit; **node1**, **node2**... are subcircuit's external nodes; **parm1**, **parm2**... are parameters of the subcircuit and separated by space or comma. Subcircuits having the same circuit structure

but different parameters only need one subcircuit definition. After **.subckt** card, there are a series of element cards which describe the subcircuit structure. Subcircuit should use **.ends** card to finish its definition. (See following) No control cards and options cards are allowed within a subcircuit definition. However nested subcircuit definition is possible. Any nodes in subcircuit definition except those in **.subckt** card are considered as local. Ground node is always global.

## 7.2 Subcircuit end card

General form:

**.ends subnam**

Example:

.ends opamp

This card should be the last line of any subcircuit definition. **subnam** denotes the subcircuit name.

## 7.3 Subcircuit call

General form:

**xyyyyyy node1 [ node2 node3 ...] subnam [(parm1 [parm2 parm3 ...])]**

Examples:

x1 3 0 2 4 opamp (800k 100, 1e5)

xa 1 2 3 block1

SCNAP5 treats subcircuit as a pseudo element. **node1**, **node2**... are nodes which connect to the subcircuit. **subnam** represents the subcircuit name, followed by a series of parameter values. The node and parameter sequence should be the same as defined in corresponding **.subckt** card. If the user wants to reference an element in a subcircuit, the element name should be written as follows; from left to right, first the element name, followed by an underline, then the name of subcircuit call. For example, **c1** is in a subcircuit named **opamp** and the subcircuit call is **x1**. To reference **c1**, one should write it as **c1_x1**. If there are nested subcircuits, then write all subcircuit calls from inside to outside with an underline between each. eg. **e1_xa_xb_xc** .

## 8. Analyse control description

SCNAP5 supports time-domain analysis for both switched capacitor circuits, switched current circuits and continuous time circuits.

General form:

**.tran tstart tstop tstep**

Examples:

.tran 0 5ms 0.03ms

.tran 0 3200us 16us

**tstart** is the time at which the analysis is to start and must be greater than or equal to zero. **tstop** is the time at which the analysis is to stop and must be greater than **tstart**. **tstep** is the printing or plotting increment. **tstep** should be greater than zero.

## 9. Option facilities

General form:

**.options opt1 opt2... (or opt=optval...)**

Examples:

.options ron = 10 ohm

The above card means that all switch-on resistances are set to 10 ohm. SCNAP5 allows user to select following options in an arbitrary order.

| options | function |
|---|---|
| **order = x** | specify approximation order of input source for transient analysis (default is 5) |
| **roff = x** | set switch-off resistances which have not been specified in switch cards. (default 1E10 ohm) |
| **ron = x** | set switch-on resistances which have not been specified in switch cards. (default 1 ohm) |
| **acct** | print out the run time statistics. |

## 10. Sample and hold

General form:

**.sample input clknam**

**.sample output clknam**

Examples:

.sample output clk2

.sample input clk1

SCNAPDIS allows users to study sample and hold effects for both input signal and output response. **input** and **output** are key words and refer to signal type. **clknam** is the clock name which describes sample and hold time intervals. These time intervals correspond to certain basic time slots. For input signals, it means that input is only supplied in defined clock phases. Similarly, for output sample and hold effect, the outputs are only observed in defined clock phases.

## 11. Plot card

General form:

**.plot pltype ov1 < ov2...>**

Example,

.plot tran v(2) v(3) i(vin#branch)

After each successful run, an output file named rawfile will be created automatically. It is in the same format as produced by SPICE3. So it directly fits into SPICE post-processor NUTMEG. **pltype** denotes the required analysis type. (transient in this case) For transient analysis, the output variable types are node voltage and branch current. To reference a branch current, the branch name should be formed correctly. For most of the elements, it is the combination of an element name, which produces the branch current, and "#branch" . For current-controlled voltage source, "#contbranch" is needed to reference its controlling branch.

## 12. Examples

Several circuits are used to show various facilities of SCNAP5.

A) Fully balanced first-order sigma-delta SC modulator

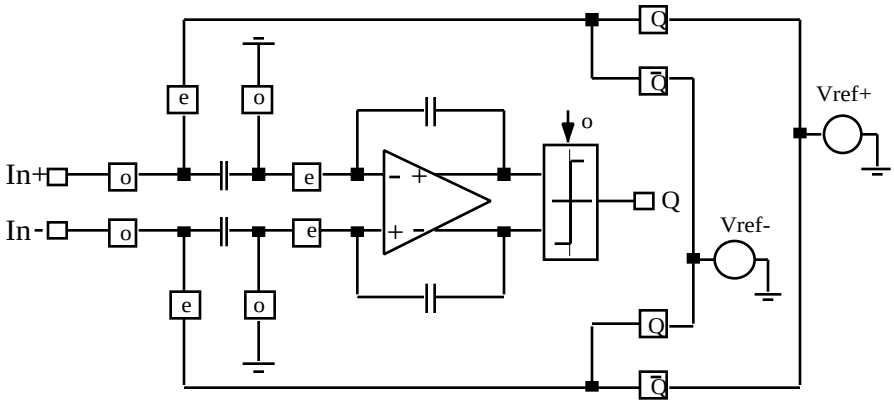



Fig. 2 First-order sigma-delta SC modulator

The following is the SCNAP5 circuit description file,

```
* First-order sigma-delta modulator
* scnap5 netlist
*
•  periodically controlled switches
```

```
s1 1 6 phi1
s6 6 11 phi2
s7 7 0 phi1
s8 7 8 phi2

s2 2 3 phi1
s3 3 12 phi2
s4 4 0 phi1
s5 4 5 phi2

* feed back controlled switches
s9 11 100 clk1
s10 11 200 clk2
s11 12 100 clk2
s12 12 200 clk1

* reference voltage
vref- 100 0 dc -1v
vref+ 200 0 dc +1v

* sampled capacitors
c3 6 7 0.5pf
c1 3 4 0.5pf

* integrator capacitors
c4 8 9 1.0pf
c2 5 10 1.0pf

* opamps
e2 5 8 9 0 50k
e1 9 0 10 0 -1

* comparator
k1 9 10 99 phi1

* switching rate = 1.66666667MegHz
.phase phi1 pwl 0u 1v 0.3u 0v 0.6u 1v
.phase phi2 pwl 0u 0v 0.3u 1v 0.6u 0v

* feed back clock signal
.phase clk1 d2a 0u 0v 0.3m 5v
.phase clk2 d2a 0u 0v 0.3m 5v

* a2d node
.a2d 99999 99 0v 5v 0us

* d2a node (never used)
.d2a 99998 clk1 0v 5v 0.0us 0.0us
.d2a 99997 clk2 0v 5v 0.0us 0.0us

* input
v1 1 0 dc -0.5
v2 2 0 dc 0.5

* print out job statistics
.option acct

* analyse control
```

```
.tran 0u 30u 0.3u
.plot tran v(99999) v(9) v(10) v(11) v(12)
.end
```

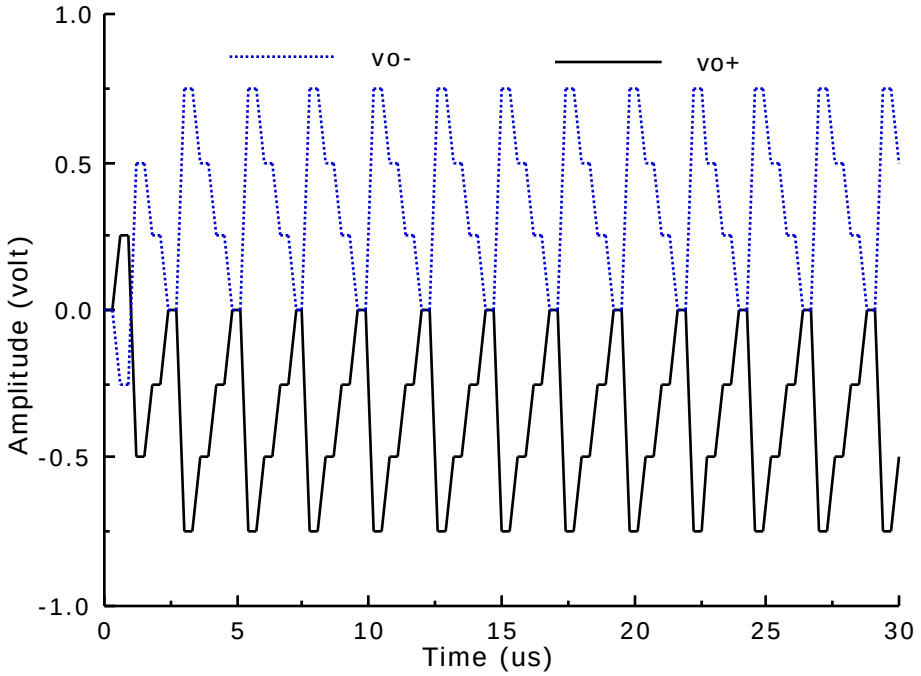



**Fig. 3.1 Output waveform of balanced opamp of a 1st-order sigma-delta A/D converter**

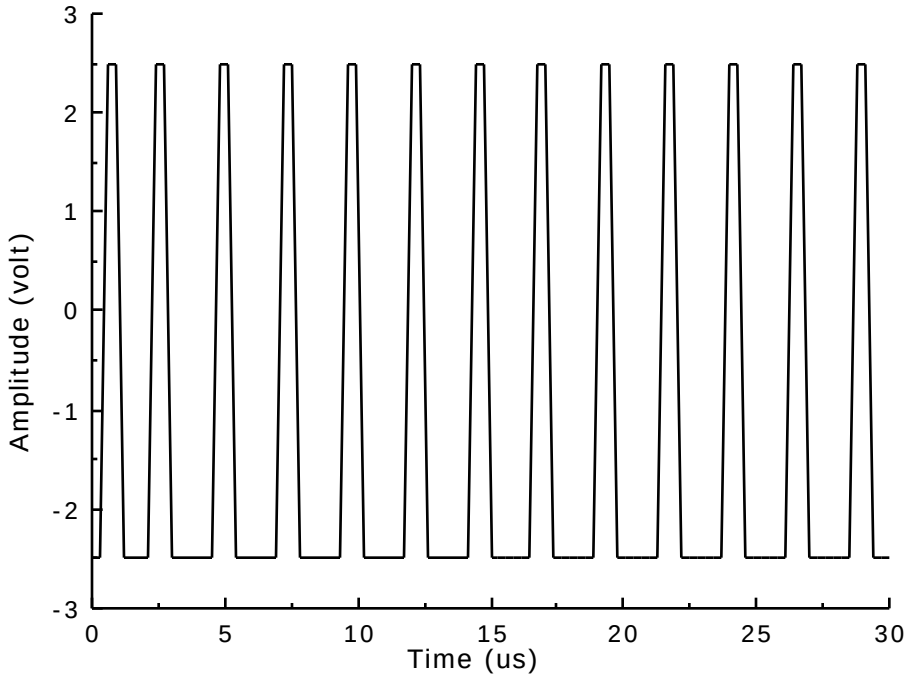



**Fig. 3.2 Output waveform of the comparator of a 1st-order sigma-delta A/D converter**

B) A 2nd-order sigma-delta SC modulator

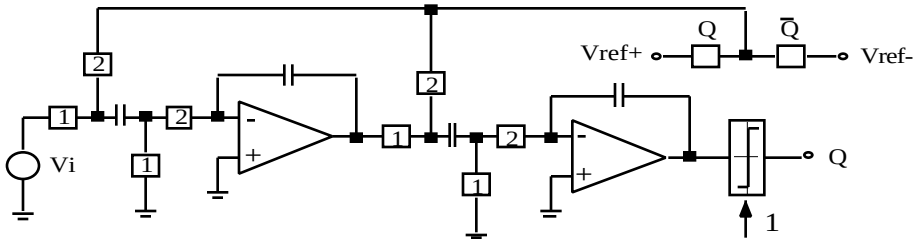



Fig. 4 SC implementation of a second-order sigma-delta modulator

The netlist is given as follows,

```
* second-order sigma-delta modulator
* scnap5 netlist
*
* input frequency = 1kHz
vin 1 0 sin 0 0.5v 1kHz

* periodically controlled switches
s1 1 2 phi1
s2 2 11 phi2
s3 3 0 phi1
s4 3 4 phi2
s5 5 6 phi1
s6 6 11 phi2
s7 7 0 phi1
s8 7 8 phi2

* feed back controlled switches
s9 11 100 clk1
s10 11 200 clk2

* sampled capacitors
c1 2 3 0.5pf
c3 6 7 0.5pf

* integrator capacitors
c2 4 5 1.0pf
c4 8 9 1.0pf

e1 0 4 5 0 1e3
e2 0 8 9 0 1e3

* comparator
k1 0 9 99 phi1
```

```
* switching rate = 1.66667MegHz
.phase phi1 pwl 0u 1v 0.3u 0v 0.6u 1v
.phase phi2 pwl 0u 0v 0.3u 1v 0.6u 0v

* feed back clock signal
.phase clk1 d2a 0u 0v 0.3m 5v
.phase clk2 d2a 0u 0v 0.3m 5v

* a2d node
.a2d 99999 99 0v 5v 0us

* d2a node (never used)
.d2a 99998 clk1 0v 5v 0.0us 0.0us
.d2a 99997 clk2 0v 5v 0.0us 0.0us

* reference voltage
vref+ 100 0 dc 1v
vref- 200 0 dc -1v

* print out job statistics
.option acct ron=1

* analyse control
*.tran 0u 4.0e-2 0.3u
.plot tran v(99)
.end
```

N. B. FFT routines are required to produce the following graphs. A considerable amount of computer time is required to produce Fig. 4.1!

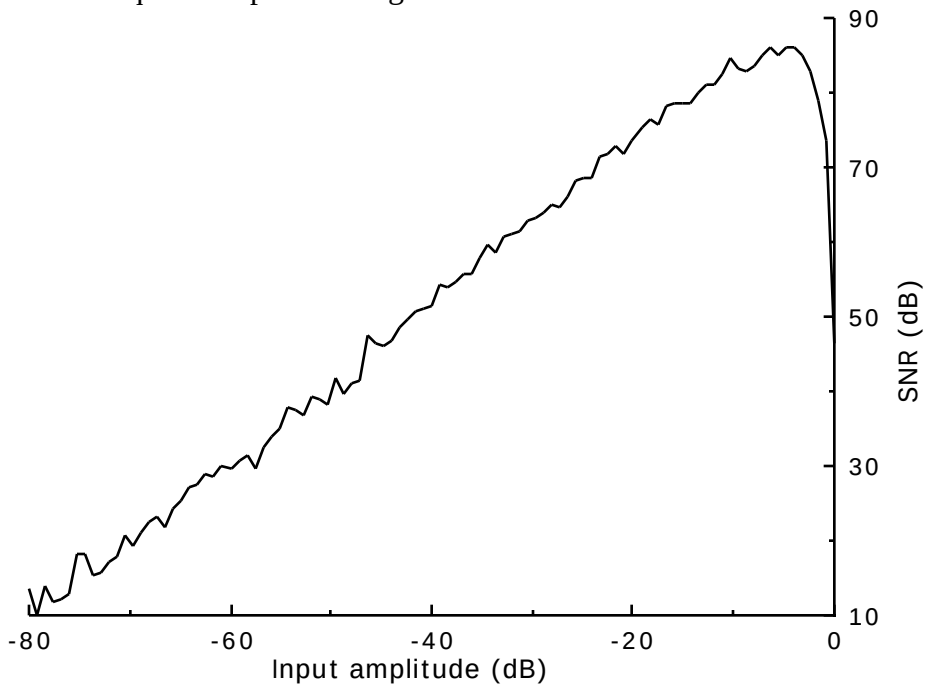



**Fig. 4.1 SNR versus relative input amplitude for 2nd-order sigma-delta modulator**

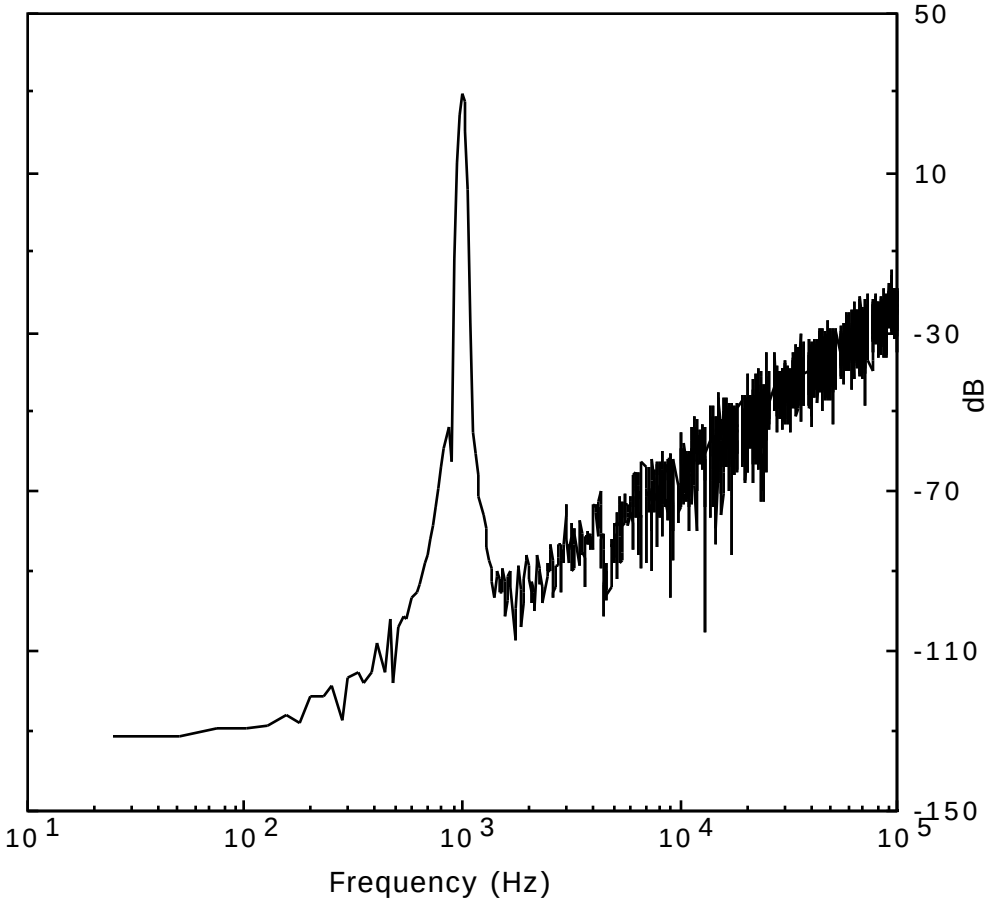



**Fig. 4.2 FFT spectrum of the comparator output for 2nd-order sigma-delta modulator**

The commands of in house software to produce FFT and SNR curves are as follows,

*sim c_fft 64K 1.6666666667M NUTTALL 0 < sdmout*

*sim c_snr 64K 1k 1.66666666667M 3.90625E-3 NUTTALL 0 < sdmout*

C) 5th-order elliptic lowpass SC filter

SCNAP5 can also analyse periodic sampled-data analogue circuits.

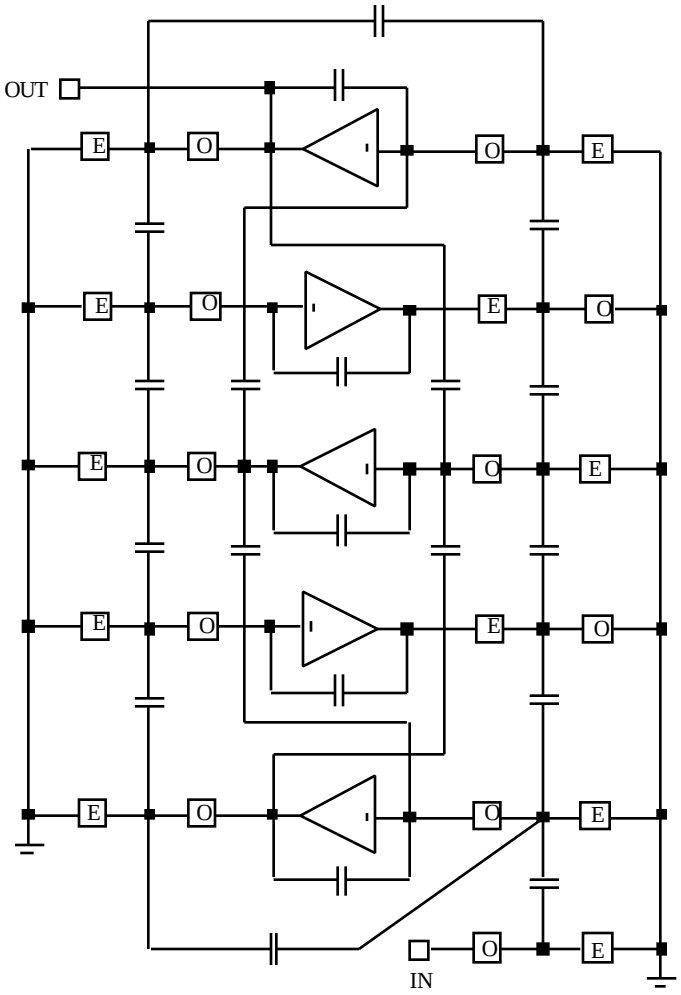



Fig. 5 5th-order elliptic lowpass SC filter

The circuit description file is,

```
5th order elliptic lowpass

.option acct
c1 3 4 27.3p
c2 2 3 30.2p
c3 5 6 79.2p
c4 4 7 10.9p
c5 8 9 50.6p
```

```
c6 3 10 35.7p
c7 7 11 10p
c8 6 12 10p
c9 12 13 146p
c10 5 13 10p
c11 10 14 32.7p
c12 11 15 16.7p
c13 12 21 19p
c14 13 20 15.8p
c15 14 18 29.2p
c16 16 17 59.5p
c17 15 19 10p
c18 20 21 30.8p
c19 18 22 21.1p
c20 19 22 10p

s1 1 2 even
s2 2 0 odd
s3 3 0 odd
s4 10 0 even
s5 14 0 odd
s6 18 0 even
s7 22 0 odd
s8 4 0 odd
s9 7 0 odd
s10 11 0 odd
s11 15 0 odd
s12 19 0 odd
s13 4 5 even
s14 7 8 even
s15 11 12 even
s16 15 16 even
s17 19 20 even
s18 3 6 even
s19 9 10 odd
s20 13 14 even
s21 17 18 odd
s22 22 21 even

e1 0 21 20 0 100k
e2 0 16 17 0 100k
e3 0 13 12 0 100k
e4 0 8 9 0 100k
e5 0 6 5 0 100k

vin 1 0 pulse -1 1 0 8u 8u 984us 2ms

.phase even pwl 0us 5v 8.0us 0v 16.0us 5v
.phase odd  pwl 0us 0v 8.0us 5v 16.0us 0v

.tran 0 3.992m 8u
.plot tran v(20) v(1)

.end
```

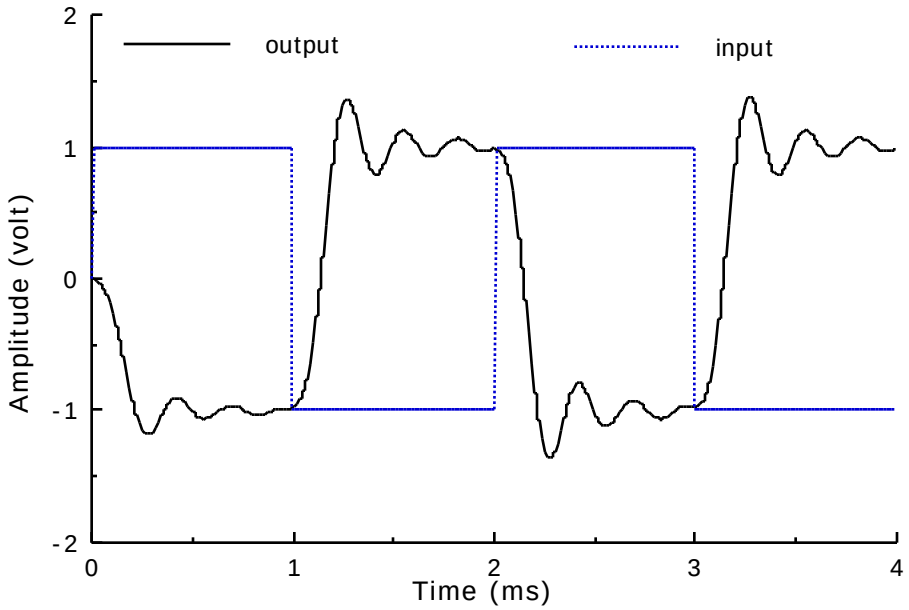



**Fig. 5.1 Input and output waveform of 5th order filter**

## References

[1] Z. Q. Shang and J. I. Sewell, "SCNAP4 User's Guide (version 1.9)", Department of Electronics and Electrical Engineering, University of Glasgow, 1999

[2] "Analog Artist Design System SPICE Socket for Mixed Signal", Analog Artist Version A2.4 Pre-Release, Cadence Design Systems, Inc., May 1, 1991

[3] Z.Q.Shang and J.I.Sewell, “Development of efficient switched network and mixed-mode simulators”, Proc. IEE - Circuits, Devices and Systems, vol. 145, no. 1, February 1998, pp. 24-34